UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S)	Humblet, Pierre	GROUP ART UNIT:	2734
APPLN. NO.:	09/051,687	EXAMINER:	Temesghen Ghebretinsae
FILED:	10/10/2000	CONF. NO.	8289
TITLE:	DIGITAL-TO-ANALOG COMMUNICATION DEVICE AND METHOD		

APPEAL BRIEF

Electronically Filed

Sir:

This Appeal Brief is being filed Dec.21, 2006 as a follow up to a Notice of Appeal filed on October 27, 2006. Applicant believe that no fee for an Extension of Time is needed.

Please charge any fees that may be due to Deposit Account 502117, Motorola, Inc.

Respectfully submitted,

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1) Real Party in Interest

The real party in interest for this patent application is Motorola, Inc., a corporation of the state of Delaware, having headquarters at 1303 East Algonquin Road, Schaumburg, IL 60196.

2) Related appeals and interferences

There are no appeals or interferences that are known to relate to this patent application.

3) Status of Claims

Claims 1, 2, and 12-16 stand rejected. Claims 3-10 stand as being objected to. Claim 11 has been cancelled.

Independent claims 12, 13, and 16 are being appealed.

For arguments, claims are grouped as 12, 13, and 16.

4) Status of Amendments

The Advisory Action mailed on Sept. 18, 2006 entered the amendment after final filed electronically on August 28, 2006.

5) Summary of Claimed Subject Matter

a) Independent claim 12

i) An analog adapter (FIG. 4, element 6) is a modem for connection to an analog link (FIGS 1 and 4, element 8) of a communication system.

ii) A digital adapter (FIGS. 1 and 3, element 5) is a modem for connection to a digital link (FIGS. 1 and 3, element 7) of a communication system.

iii) The communication system (FIG. 1, element 1) includes a digital exchange (FIG. 1, element 3) and an analog exchange (FIG. 1, element 4). These are well known elements of a telephone network. The analog adapter and digital adapter exchange information over the communication system.

iv) A succession of groups of bits are taken from digital information originating from a data source (FIGS. 1 and 4, element 35) connected to the analog adapter. (SPEC page 5, lines 17-29; SPEC page 8, line 18 to page 9, line 2)

v) A succession of analog signals is generated (FIG. 4, line coder 27, predistortion filter 24, D/A converter 26, and filter 25 , synchronized (element 23) to a clock of the digital adapter. (SPEC page 5, lines 17-29; SPEC page 8, line 18 to page 9, line 2)

vi) Each analog signal has an amplitude corresponding to a digital value of one of the groups of bits. The successive analog signals interfere with one another, forming a resulting analog signal at an analog interface (FIG. 1, element 8) of an analog exchange (FIG. 1, element 4) of the communication system. Each analog signal has a shape such that, at the moment when the analog signal that results from the interfering successive analog signal is sampled in the analog interface of the exchange, the resulting analog signal is substantially equal to the sum of a value determined by the digital information and of the echo of a signal being transmitted by the digital adapter, without said value having to be equal to a level of the quantization law, so that following the sampling of the resulting analog signal, a byte appears in the digital adapter (5), representing said sum. (SPEC page 5, lines 17-29; SPEC page 8, line 18 to page 9, line 2).

b) Independent Claim 13

i) An analog adapter (FIG. 4, element 6) is used in a communication system (FIG. 1, element 1) by being linked to an analog exchange (FIG. 1, element 4) by means of an analog interface (FIGS 1 and 4, element 8)

ii) a digital adapter (FIGS. 1 and 3, element 5) of the communication system may be linked to a digital exchange (FIG. 1, element 3) by means of a digital interface (FIGS. 1 and 3, element 7)

iii) the analog adapter includes at least a means (FIG. 4, element 15) for receiving digital information from the digital adapter (5) being sent to the analog adapter (6) at a rate of at least 8000 digital information bearing symbols per second (SPEC page 9, lines 7 to 14) wherein said means (15) forms a portion of the analog adapter (6) and includes an adaptive linear equalizer (FIG. 4, element 17; SPEC page 10, lines 17-18) that forms a partial response output (SPEC page 4, lines 4-8 and page 11, lines 1-3).

c) Independent Claim 16

i) analog adapter apparatus (FIG. 4, element 6)

ii) means for taking a succession of groups of bits from digital information originating from a data source (FIG. 1 and FIG. 4, element 35) connected to the analog adapter system (unnumbered buffer in FIG. 4 to which the terminal 35 is coupled), each group of bits representing an item of the digital information to be transmitted to the digital adapter;

iii) means for generating a succession of analog signals synchronized to a clock of the digital adapter (FIG. 4, elements 27, 24, 26, 25) , wherein each analog signal has an amplitude corresponding to a digital value of one of the groups of bits, wherein the successive analog signals interfere with one another, forming a resulting analog signal at an analog interface of an analog exchange of a communication system, and have a shape such that, at the moment when said resulting analog signal is sampled in the analog interface of the exchange, said resulting analog signal is substantially equal to the sum of a value determined by the digital information and of the echo of a signal being transmitted by the digital adapter (5), without said value having to be equal to a level of the quantization law, so that following the sampling of the

resulting analog signal, a byte appears in the digital adapter (5), representing said sum (SPEC page 5, lines 17-29; SPEC page 8, line 18 to page 9, line 2).

6) Grounds of Rejection to be reviewed on Appeal

a) Independent Claim 12

i) Claim 12 was rejected under 35 U.S.C. §112, second paragraph in the Final Office Action dated June 29, 2006. The examiner's entire explanation of the rejection was "Claim 12 is unclear as written". The applicant believes it is clearly stated.

ii) Claims 12 and 16 both include the description "a succession of analog signals synchronized to a clock of the digital adapter". The applicant believes this aspect is not described in the cited 35 U.S.C. § 102 prior art (U.S. 5,528,625 Ayanoglu et al.).

iii) Claims 12 and 16 both include the description: "said resulting analog signal is substantially equal to the sum of a value determined by the digital information and of the echo of a signal being transmitted by the digital adapter (5), without said value having to be equal to a level of the quantization law, so that following the sampling of the resulting analog signal, a byte appears in the digital adapter (5), representing said sum." The applicant believes that this aspect is not described in the cited 35 U.S.C. § 102 prior art (U.S. 5,528,625 Ayanoglu et al.).

b) Independent Claim 13

i) Claim 13 was rejected under 35 U.S.C.§112 second paragraph for the phrase "the digital adaptor" not having clear antecedent basis. The applicant believes this was corrected by changes entered from the amendment after final filed August 28, 2006, and conclude that it is not a ground to be reviewed on Appeal, although the applicant has no confirmation of this.

ii) Claim 13 states: "…wherein said means (15) forms a portion of the analog adapter (6) and includes an adaptive linear equalizer that forms a partial response output." The applicant believes this is not described in the cited 35 U.S.C. §102 prior art (U.S. 5,528,625 Ayanoglu et al.).

iii) Claim 13 states "…receiving digital information from the digital adapter (5) being sent to the analog adapter (6) at a rate of at least 8000 digital information bearing symbols per second…" The applicant believes this is not described in the cited 35 U.S.C. §102 prior art (U.S. 5,528,625 Ayanoglu et al.).

c) Independent Claim 16

i) Claim 16 was rejected under 35 U.S.C.§112 second paragraph for the phrase "the communication system" not having clear antecedent basis. The applicant believes this was corrected by changes entered from the amendment after final filed August 28, 2006, and conclude that it is not a ground to be reviewed on Appeal, although the applicant have no confirmation of this.

ii) The issues for independent claim 16 are the same as those for independent claim 12, but for the reasons for the 35 U.S.C.§112 second paragraph rejection.

7) Arguments

a) Independent Claim 12

i) With reference to the 35 U.S.C. §112, second paragraph rejection, Claim 12 was rejected for "being unclear as written". No further guidance was provided by the examiner, except in an interview after the filing of the Notice of Appeal. As the applicant best understood the examiner, the examiner stated that he would give no weight to the aspects of the claim that describe the aspects of the shape given to the analog signals. The applicant believes the statement clearly states a specific operational requirement of the analog adaptor.

ii) Claims 12 and 16 both include the description "a succession of analog signals synchronized to a clock of the digital adapter". The examiner asserts in the Advisory Action that, "[r]egarding claims 12 and 16[,] Ayanoglu et al. does disclose an analog adapter apparatus comprising means for taking a succession of groups of bits from the digital information originating device connected to the analog adapter and means for generating a succession of analog signals synchronized to the clock of the digital adapter (see fig .7)". The applicant believes that FIG. 7 does not show any clock recovery function that would be required for such synchronization. The applicant notes that Ayanoglu et al.'s describes modems that in today's terminology would be called analog modems that initiate analog signals that are ultimately received by another like analog modem, in which the transmitter and receiver of each analog modem operate asynchronously with reference to each other and asynchronously with reference the digital domain of the telephone network. Applicant's analog adaptor receives signals on the analog link that are generated by applicant's digital modem that operates within the digital domain of the telephone network and applicant's analog adaptor synchronizes to the clock of the digital adaptor using the received signals, to generate the signals transmitted on the analog link.

iii) Claims 12 and 16 both include the description: "said resulting analog signal is substantially equal to the sum of a value determined by the digital information and of the echo of a signal being transmitted by the digital adapter (5), without said value having to be equal to a level of the quantization law, so that following the sampling of the resulting analog signal, a byte appears in

the digital adapter (5), representing said sum." The examiner has not cited this description nor where the examiner believes it to be described in Ayanoglu et al. The applicant believes that Ayanoglu et al. do not describe this aspect. Ayanoglu et al in fact describes that the received signal at the analog to digital converter (the equivalent to the input portion of applicant's digital adaptor) must specifically be a quantization level (Ayanoglu et al. at least at col. 2, line 45 and col. 5, line 36).

b) Independent claim 13

i) Claim 13 states: "…wherein said means (15) forms a portion of the analog adapter (6) and includes an adaptive linear equalizer that forms a partial response output." The applicant believes that the examiner referred to FIGS. 6A and 6B during the interview that took place after the Notice of Appeal was filed. Applicant believes that the functions presented in FIGs. 6A or 6B, or the descriptions thereof, do not represent an adaptive linear equalizer that forms a partial response output, nor does the applicant believe that Ayanoglu et al. describes the use of partial response signals or filters in the transmission portion of the analog modems described therein.

ii) Claim 13 states "…receiving digital information from the digital adapter (5) being sent to the analog adapter (6) at a rate of at least 8000 digital information bearing symbols per second…" The applicant believes this is not described in the cited 35 U.S.C. §102 prior art (U.S. 5,528,625 Ayanoglu et al.). Ayanoglu et al. clearly describes a system in which 6000 digital information bearing symbols are used, each carrying a value selected from 256 values. In particular, Ayanoglu et al. at column 8, lines 3 to 8, clearly states a conclusion that using more than 6 ksymbols/sec. is theoretically not possible. At column 7, lines 15-29, Ayanoglu et al. explicitly describes the use of 6ksymbols/sec of information bearing symbols.

c) Independent claim 16

i) The arguments for independent claim 16 are the same as the arguments presented in claim 12 under Section 7) a) ii) and 7) a) iii).

8) Claims Appendix

1. A communication system for communicating digital information, the communication system comprising a digital adapter (5) and an analog adapter (6), wherein the digital adapter (5) is linked to a digital exchange (3) by means of a digital interface (7) and the analog adapter (6) is linked to an analog exchange (4) by means of an analog interface (8), said exchanges (3,4) being linked by means of a telecommunications network (2), wherein said digital adapter and analog adapter include link means (11,12;15,16) for linking between the digital adapter (5) and the analog adapter (6), the digital information from the digital adapter (5) being sent to the analog adapter (6), and vice versa, in a digital form without emulating an analog signal.

2. A system according to claim 1, wherein said link means (11,12;15,16) include, in the direction of transmission going from the digital adapter (5) to the analog adapter (6), a digital transmitter (11) situated in the digital adapter (5) and able to transmit, to an analog receiver (15) situated in the analog adapter (6), analog pulses the voltage levels of which represent the digital information transmitted from the digital adapter (5) to the analog adapter (6).

3. A system according to claim 1, wherein said link means (11,12;15,16) include, in the direction of transmission going from the analog adapter(6) to the digital adapter (5), an analog transmitter (16) situated in the analog adapter (6) and able to transmit, to a digital receiver (12) situated in the digital adapter (5), an analog signal such that, when the analog signal is sampled by the analog interface of the exchange (4), the sample of the analog signal will equate to the sum of a value able to be determined by the digital information transmitted by the analog adapter (6) to the digital adapter (5) and of the echo of the signal transmitted by the digital adapter (5), without said value having to be equal to a level of a quantization law.

4. A system according to claim 1 or claim 2, wherein the receiver of the analog adapter (6) includes an adaptive linear equalizer (17) connected at its input to the output of an analog/digital converter (19), and connected at its output to the input of an output equalizer (20) linked to the user's equipment, so that the response at the output of the adaptive linear equalizer (17) is a partial response, in particular a class IV response.

5. A system according to claim 4, wherein said partial response is determined adaptively.

6. A system according to claim 4 or claim 5, wherein said output equalizer (20) is a decision feedback equalizer or a Viterbi equalizer.

7. A system according to claim 1 or claim 2, wherein said means (11, 12) include, at the digital adapter (5) end, an n-level selector (14), n being equal, particularly, to 64, said levels being represented in the form of a byte, from among N = 256 possible quantization levels, said level selector (14) being connected, at its input, to the user's equipment and, at its output, to a digital interface.

8. A system according to claim 3, wherein said transmitter (16) of the analog adapter (6) includes a line coder (27) followed by a predistortion filter (24) which synthesizes a partial response, in particular a class IV response.

9. A system according to claim 8, wherein said partial response is determined adaptively.

10. A system according to claim 1 or claim 3 wherein the digital adapter (5) includes a decoder (30) connected, at its input, to an echo filter (22) and to the output of the digital interface of the digital adapter (5), said decoder (30) delivering at its output to the user's equipment (9) the most likely sequence of groups of bits transmitted by the analog adapter (6), given the echo of the signal produced by the digital adapter (5).

Claim 11 is cancelled.

12. A method of transmission from an analog adapter (6) to a digital adapter (5) in a communications system, said method including in the analog adapter the steps of:

- taking a succession of groups of bits from digital information originating from a data source connected to the analog adapter; and
- generating a succession of analog signals synchronized to a clock of the digital adapter, wherein each analog signal has an amplitude corresponding to a digital value of one of the groups of bits, wherein the successive analog signals interfere with one

another, forming a resulting analog signal at an analog interface of an analog exchange of the communication system, and have a shape such that, at the moment when said resulting analog signal is sampled in the analog interface of the exchange, said resulting analog signal is substantially equal to the sum of a value determined by the digital information and of the echo of a signal being transmitted by the digital adapter (5), without said value having to be equal to a level of the quantization law, so that following the sampling of the resulting analog signal, a byte appears in the digital adapter (5), representing said sum.

13. An analog adapter (6) for use in a communication system, wherein a digital adapter (5) of the communication system may be linked to a digital exchange (3) by means of a digital interface (7), and the analog adapter (6) may be linked to an analog exchange (4) by means of an analog interface (8), said exchanges (3,4) being linked by means of a telecommunications network (2), wherein said analog adapter includes at least a means (15) for receiving digital information from the digital adapter (5) being sent to the analog adapter (6) at a rate of at least 8000 digital information bearing symbols per second, wherein said means (15) forms a portion of the analog adapter (6) and includes an adaptive linear equalizer that forms a partial response output.

14. The device according to claim 13, wherein the information in each information bearing symbol is a group of bits originating from a digital data source and each information bearing symbol is a voltage level determined by choosing one voltage level from among a plurality of voltage levels that corresponds to the group of bits, a sequence of the voltage levels each said voltage level represented in digital form by one byte and being transmitted 8000 times per second.

15. The method according to claim 12, further comprising in the digital adapter the steps of:

- processing the successive groups of bits so as to retrieve the most likely sequence of the groups of bits, given the echo of the signal being transmitted by the digital adapter;
- transmitting the digital value of the groups of bits processed to an equipment of a user.

16. An analog adapter apparatus, comprising:

- means for taking a succession of groups of bits from digital information originating from a data source connected to the analog adapter system, each group of bits representing an item of the digital information to be transmitted to the digital adapter; and

- means for generating a succession of analog signals synchronized to a clock of the digital adapter, wherein each analog signal has an amplitude corresponding to a digital value of one of the groups of bits, wherein the successive analog signals interfere with one another, forming a resulting analog signal at an analog interface of an analog exchange of a communication system, and have a shape such that, at the moment when said resulting analog signal is sampled in the analog interface of the exchange, said resulting analog signal is substantially equal to the sum of a value determined by the digital information and of the echo of a signal being transmitted by the digital adapter (5), without said value having to be equal to a level of the quantization law, so that following the sampling of the resulting analog signal, a byte appears in the digital adapter (5), representing said sum.

9) Evidence appendix

There is no evidence that has been entered in this application.

10) Related proceedings

There are no proceedings known to be related to this application.